



Europa Orbiter/X2000 Avionics Industry Briefing



System Flight Computer

Dwight A. Geer

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June 6, 2001



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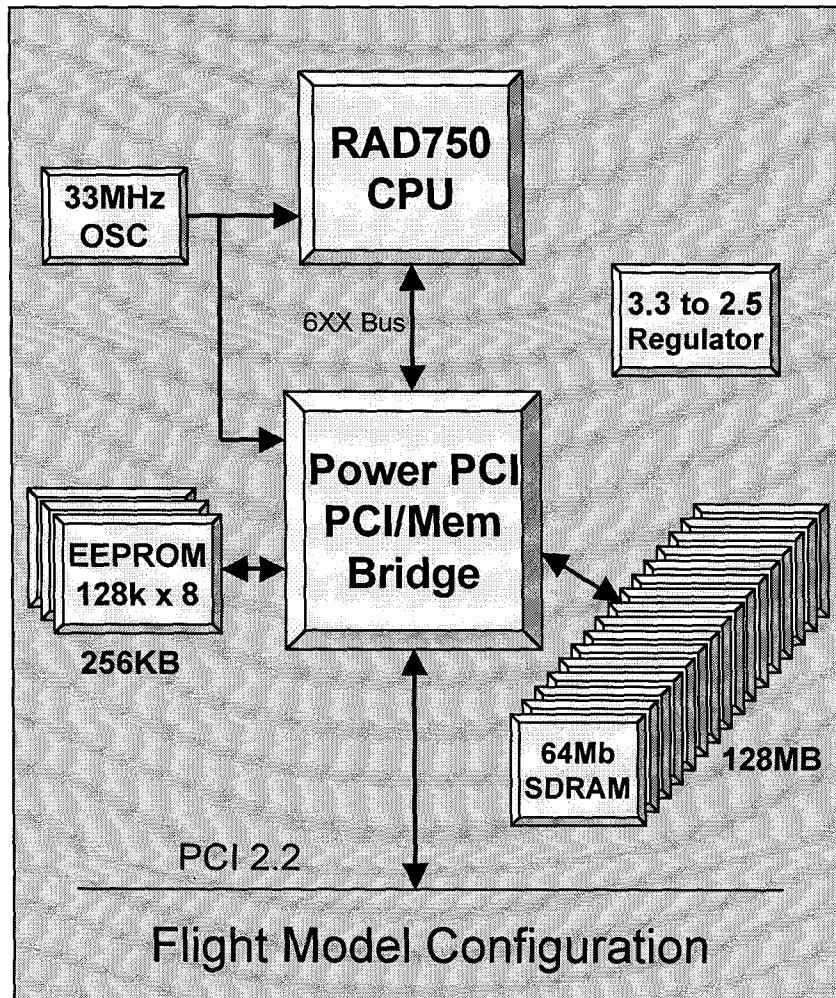


Description

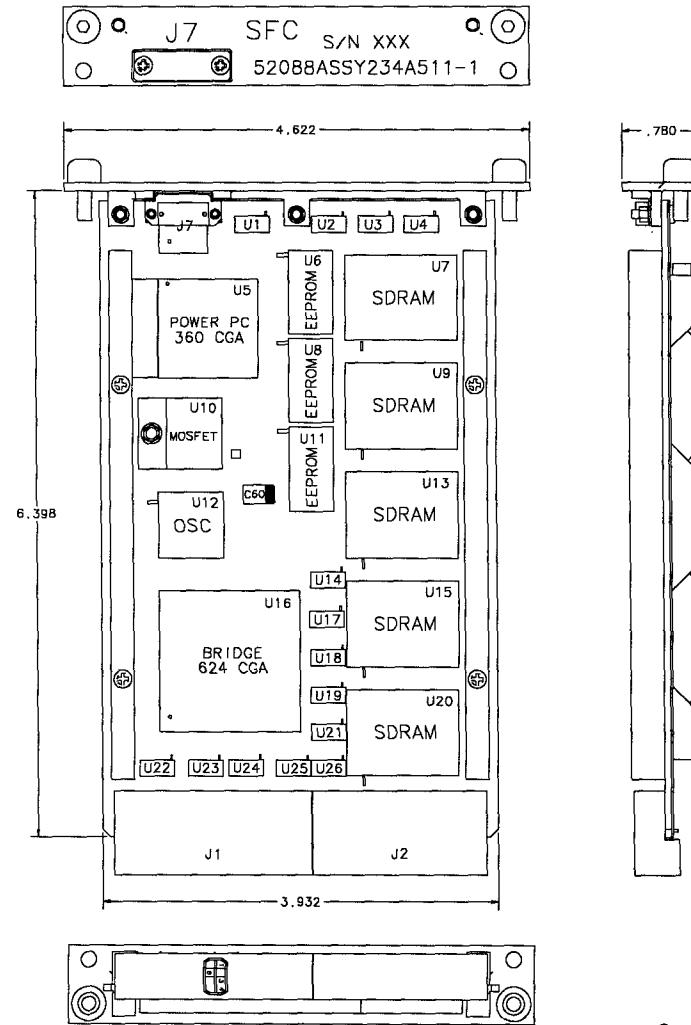
- The System Flight Computer development contract with BAE SYSTEMS, Manassas
 - Two performance versions:
 - Baseline: 33 MHz on-board oscillator (EM boards delivered)
 - Enhanced: 66 MHz on-board oscillator plus additional Power PCI functionality (new effort)
 - Commercial SFC (Prototype)
 - Engineering Model (EM)
 - Flight Model (FM)
- System Flight Computer components
 - Double-sided Compact PCI card
 - RAD750 radiation hardened PowerPC 750
 - Power PCI radhard (radiation hardened) PCI bridge chip
 - Shielded Stacked SDRAM
 - RadPack Maxwell (SEI) EEPROM
 - Radhard QTECH oscillator
 - Radhard Omnidrel linear regulator
- Interfaces
 - CompactPCI bus
 - UART Interface
 - Interrupts and Discretes – Programmable I/O Discretes
 - JTAG Interface



Block Diagram



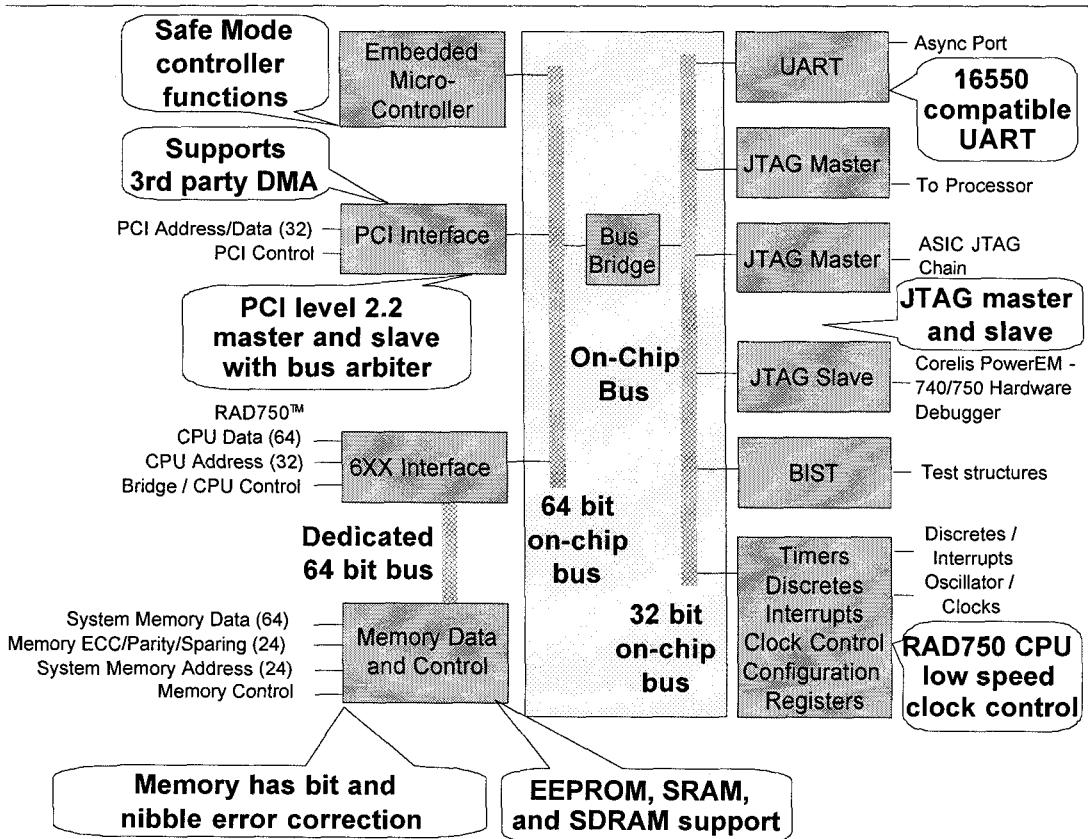
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Power PCI ASIC Description

- Power PCI provides all required on-card support functions including interfaces to:
 - PCI
 - Memory
 - CPU
 - Test equipment (UART/JTAG)



- Power PCI architecture features
 - Multiple on chip bus structure for highest throughput
 - Dedicated processor - memory bus with ECC
 - High performance processor - PCI bus with parity
 - Lower performance peripheral and test bus
 - Bit and nibble **memory error correction**
 - Clock generation and control (**System, PCI, CPU**)
 - PCI Version 2.2 **master / target and central arbiter**
 - Asynchronous PCI interface
 - **JTAG diagnostics (master and slave capable)**
 - **16550 compatible UART**
 - **Programmable interrupts and timers**
 - Error recovery embedded micro-controller function



Key Requirements

- Exceeds SPEC95 performance benchmarks (3.2 SPECint95, 2.5 SPECfp95)
 - 6.5 SPECint95, 3.9 SPECfp95 and 240 Dhrystone 2.1 MIPS
 - Performance degradation < 20% while PCI DMA activity is at 66 MB/s
- Power conservation modes controllable by software
- 32 bit 33 MHz CompactPCI Bus Specification, PCIMG 2.0 R2.1
- > 128 MBytes main memory
- > 128 KBytes (256 KBytes actual) SUROM
- EDAC mechanism for all memory
- JTAG and built-in self-test (BIST) capability
- JPL Double-Sided CompactPCI Mechanical ICD (MICD)
- Software includes:
 - Test routines to support BIST functions executed out of SUROM or RAM
 - BSP interface functions and SFC configurable hardware drivers
 - SUROM software to initialize the SFC to a known operational state

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Key Requirements

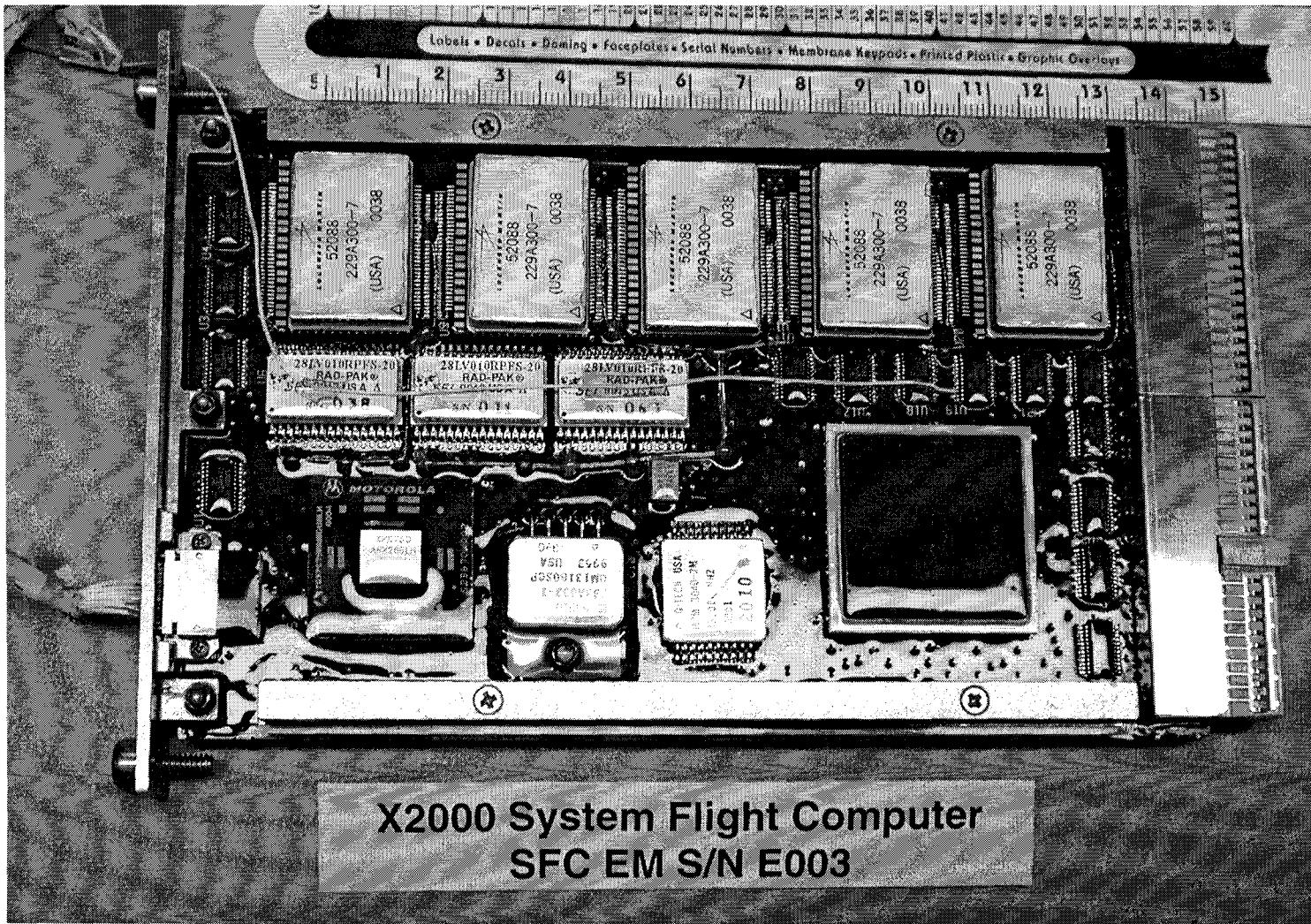
Performance		Clock Rate		PowerPC Core (2.5v)	PowerPC I/F (3.3v)	PowerPCI	DRAM	Osc's	Total (Typ)
Full Speed	242 MIPS	132	MHz	6.0	0.3	1.5	2.0	0.2	10.0
3x Speed	181 MIPS	99	MHz	4.9	0.3	1.5	1.9	0.2	8.7
2x Speed	121 MIPS	66	MHz	3.8	0.2	1.5	1.8	0.2	7.4
High	60 MIPS	33	MHz	2.6	0.2	1.5	1.6	0.2	6.1
Half	30 MIPS	17	MHz	2.1	0.1	1.3	1.3	0.2	5.0
Quarter	15 MIPS	8	MHz	1.8	0.1	1.1	1.2	0.2	4.4
Eighth	7.5 MIPS	4	MHz	1.6	0.1	1.1	1.1	0.2	4.1
Doze		132	MHz	2.4	0.1	1.0	0.5	0.2	4.2
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Doze		8	MHz	0.5	0.1	1.0	0.5	0.2	2.3
Doze		4	MHz	0.5	0.1	1.0	0.5	0.2	2.3
Nap		132	MHz	0.3	0.1	1.0	0.5	0.2	2.1
Sleep		132	MHz	0.2	0.1	0.8	0.5	0.2	1.8

SFC Mass	Line Weight		Growth Weight	
	0.549	3%	0.564	KGS
	1.207	LBS	1.241	LBS

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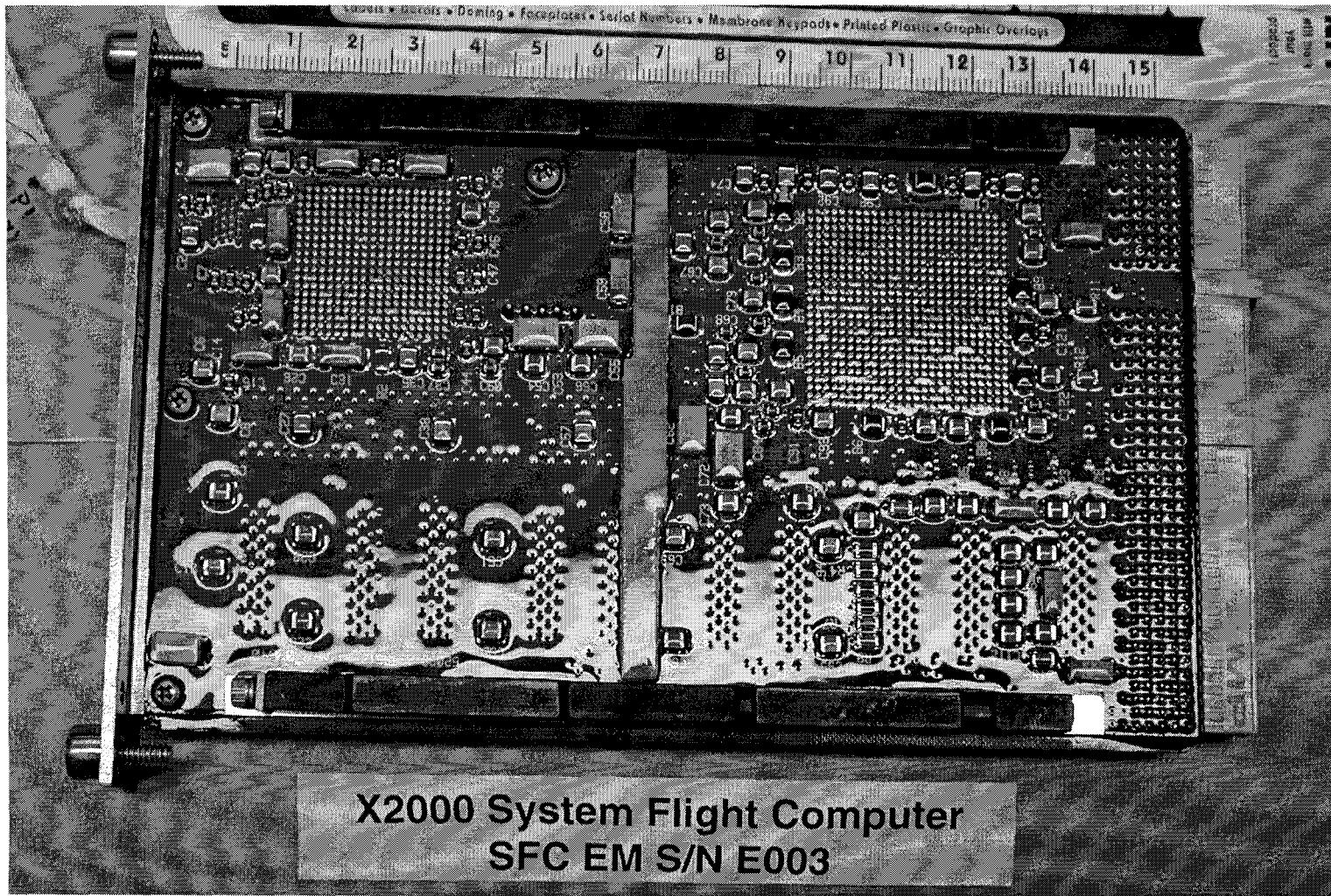
Picture of the first SFC EM



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Picture of the first SFC EM





Key Requirements – SFC Enhancement

- Power PCI internal operation at 66 MHz (baseline is 33 MHz)
 - Reduces memory latency for cache miss
- DMA Controller with the following features:
 - Executes a linked list of DMA commands in RAM.
 - Performs transfers in all combinations of PCI and RAM access (RAM → PCI, PCI → RAM, PCI → PCI, RAM → RAM)
 - Generates CPU interrupts on the occurrence of certain events
 - Example: command completion, command list completion and error
 - Interrupts are maskable (defaults to masked)

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Quarter	30 MIPS	17 MHz		2.1	0.1	2.8	1.4	0.4	6.8
Eighth	15 MIPS	8 MHz		1.8	0.1	2.6	1.4	0.4	6.3
Sixteenth	7.5 MIPS	4 MHz		1.6	0.1	2.5	1.4	0.4	6.0



Current Status

- PDR – September 1999
- CDR – August 2000
- Power PCI Tape Out (RIT) – June 2000
- First SFC EM (baseline) – December 2000
- RAD750 Tape Out (RIT) – February 2001
- EM QUAL Unit – June 2001
- Power PCI Tape Out (RIT-B) – August 2001
- First SFC FM (baseline RIT-B) – January 2002
- Power PCI (enhanced) Tape Out (RIT) – October 2002
- First SFC PT (enhanced) – January 2003
- First SFC EM (enhanced) – May 2003



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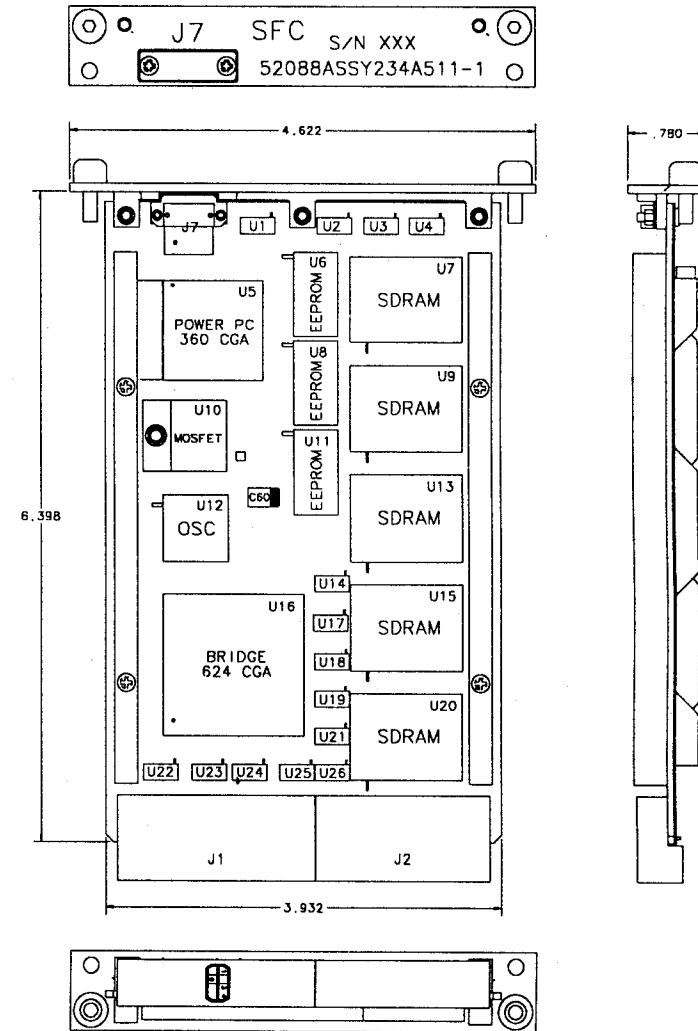
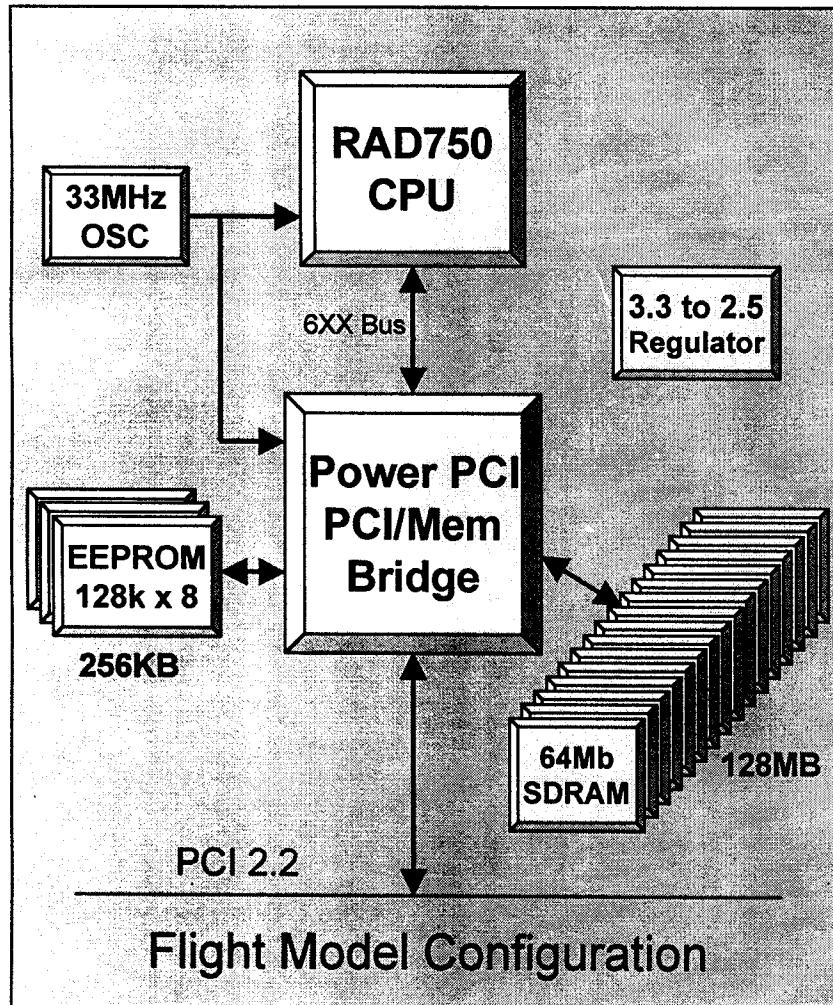


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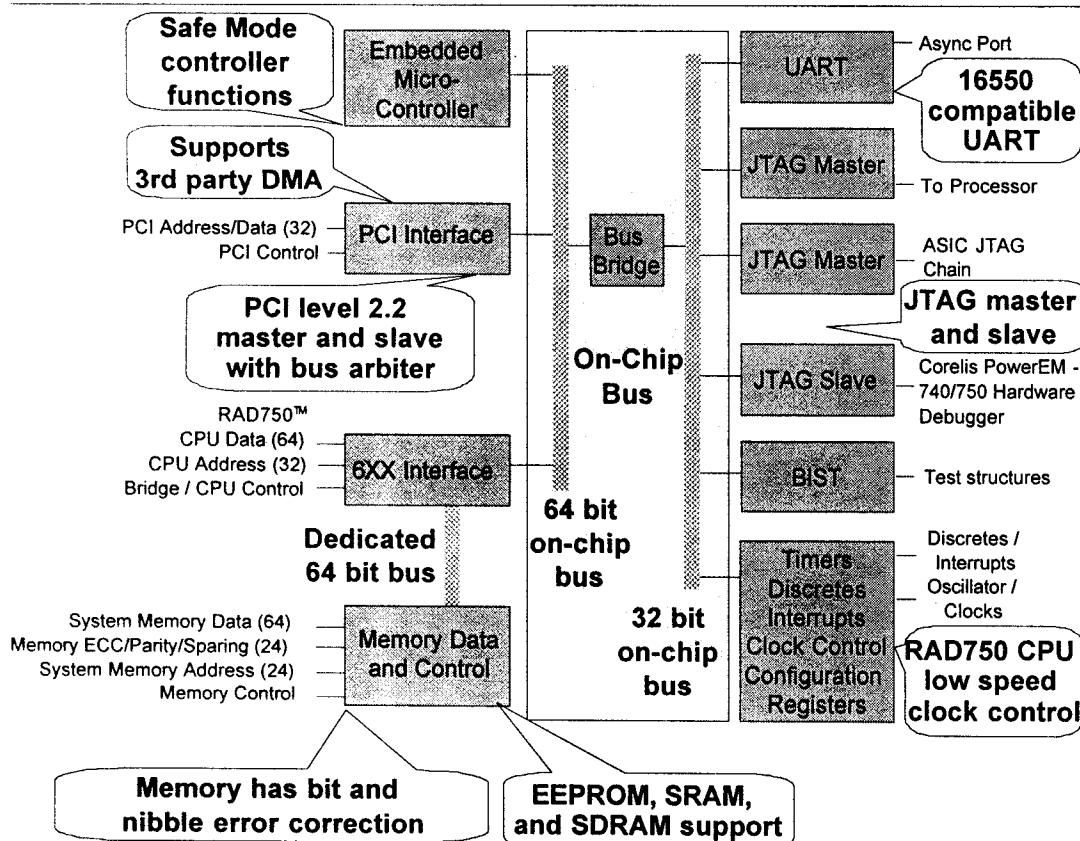
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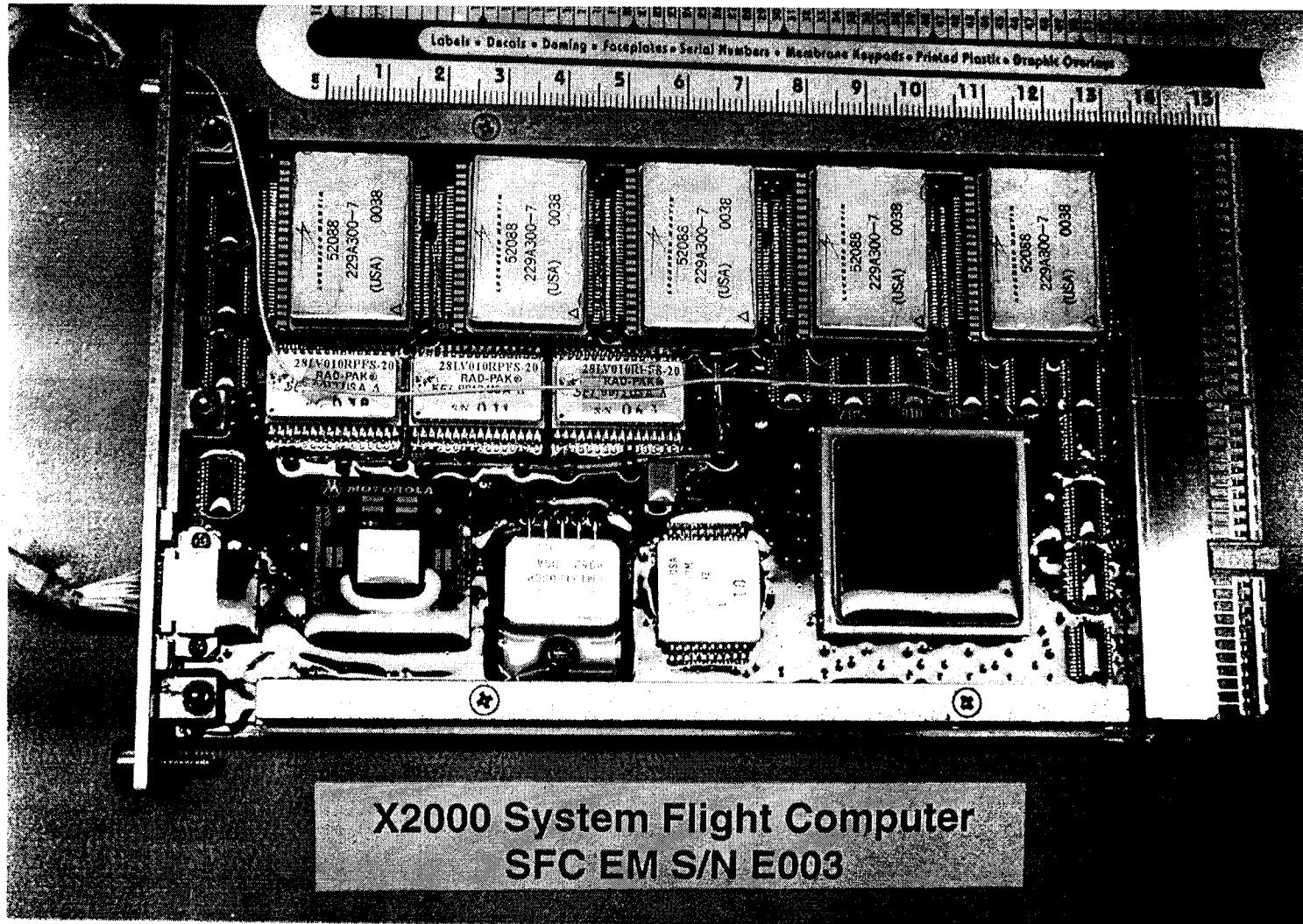
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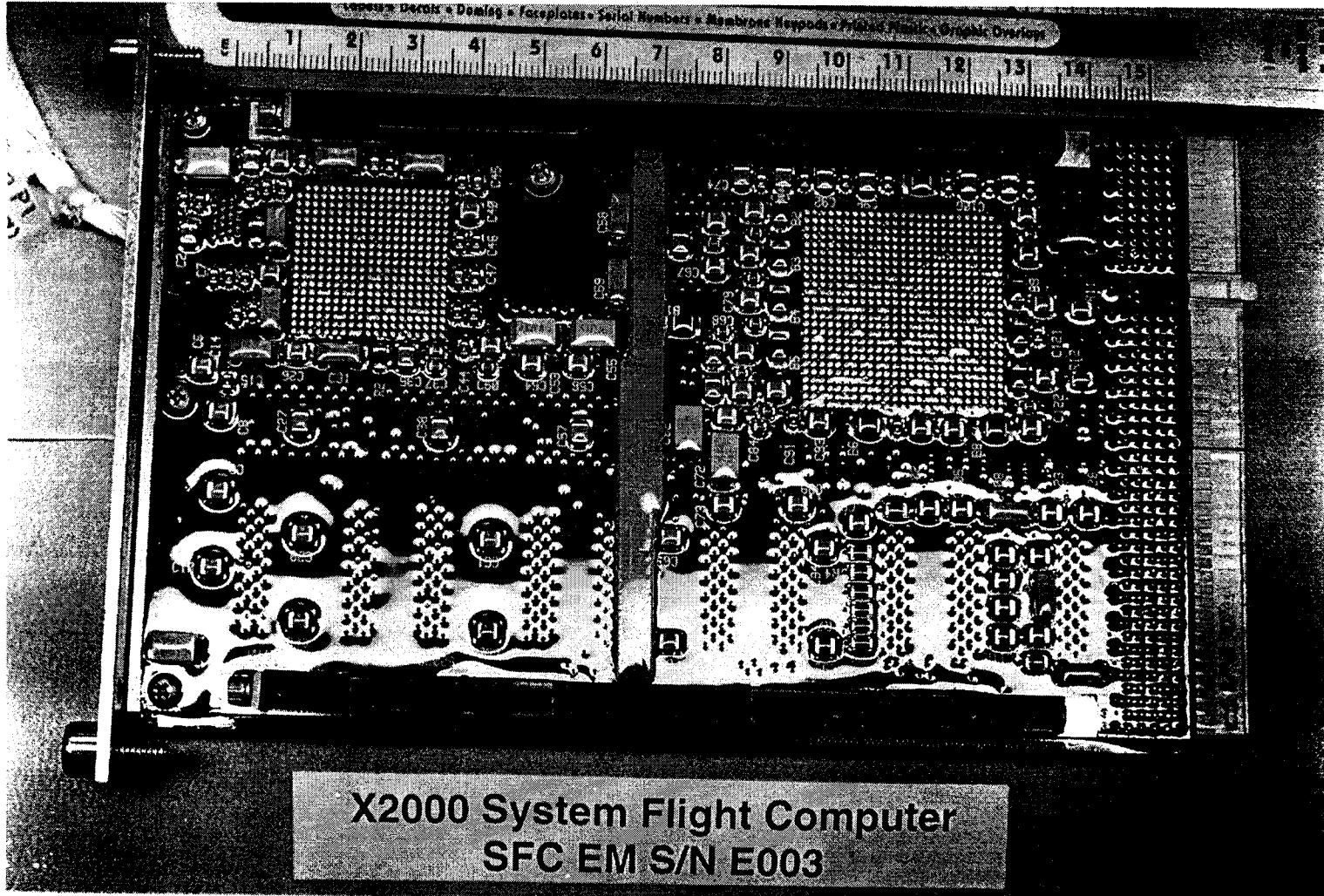


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